CURRICULUM VITAE (D.Sc. (Tech.) Tero Säntti, 07.03.2025)

Name:	Tero Antti Mikael Säntti
Date of Birth:	18 April 1974
Nationality:	Finnish
Languages:	Finnish, English, Swedish, (German, Japanese)
Maritial Status:	Common-law marriage

Academic Degrees:	D.Sc. (Tech.) in Microelectronics (Computer Systems), University of Turku, Finland, 2008 M.Sc. in Electronics and Information Technology, University of Turku, Finland, 2002
Current Positions:	Senior Engineer, Kovilta Oy, Finland, (6/2017 ->) Senior Engineer, Aboa Space Research Oy, Finland, (5/2011 ->), co-owner (3/2013 ->), Chairman of the Board (5/2021 ->) Senior Research Fellow, University of Turku, Finland (1/2017 ->)
Previous Positions:	Various positions at the University of Turku since 5/1999 On commission, Minima Processor Oy, Finland, FPGA design
Research Activities:	Since 1998 Säntti has been interested in electronic circuit design, embedded systems and system level integration. FPGA based implementations, visual data processing and content analysis are high on his list of interests. Especially focusing on the application of such systems to real life problems and applications. The applications have ranged from extracting space debris from optical images to monitoring and controlling of high-power laser welding. These far ends represent the polar opposites in terms of speed, several seconds of exposure time for the debris vs. 1000 fps for welding, and also in processing capability, high performance computers for debris vs. embedded system for welding. The space debris activities, including star catalogue matching, and the microscope activities demonstrate a wide range of targets in terms of physical size. Säntti has been involved in both experimental, pre-commercialization prototyping and commercial development.
Publications:	The D.Sc. (Tech.) thesis of Säntti was “A Co-Processor Approach for Efficient Java Execution in Embedded Systems”, University of Turku, 2008. Säntti has published 81 publications (According to Google Scholar). Additionally, he has authored several dozens of technical documents related to FPGA designs at all of the stages of a design cycle. Five selected publications: [1] *A 3D-Integrated 2-Megapixel Imager with Sparse Capture and Fine-Grain Power Gating*, International Electron Devices Meeting, 2023 [2] *Miniaturized Fluorescence Microscope for biological research in space*, International Astronautical Congress, 2021 [3] *Embedded processing methods for online visual analysis of laser welding*, Journal of Real-Time Image Processing, 2019 [4] *Design and management of image processing pipelines within CPS: Acquired experience towards the end of the FitOptiVis ECSEL Project*, Microprocessors and Microsystems, 2021 [5] *Streak detection and analysis pipeline for space-debris optical images*, Advances in Space Research, 2016